AMENDMENT(S) TO THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 12, with the following rewritten paragraph:

However, the conventional technology mentioned in Japanese Patent Publication carrying Japanese Patent No. 2694753 requires to add to the video processor a delay line dedicated to correcting the length of the signal line or an ~~a~~ electrical component such as IC for signal ling length correction, that is, for operating correction for the delay due to the signal line length. It causes a problem that its configuration becomes complicated ~~therefor~~, and its cost increases as the number of components increases.

SUMMARY ~~SUMMERY~~ OF THE INVENTION

Please replace the paragraph beginning at page 8, line 13, with the following rewritten paragraph:

As shown in FIG. 2, said delay circuit 33 is composed of a plurality of ~~buffer~~ buffers 41, which are connected in series for delaying a signal, and a selector circuit 42 for selecting an output from each buffer 41 depending on control by said control microprocessor 26 to output. Here, the plurality of ~~buffer~~ buffers 41 may be composed of connecting 100 of the ~~buffer~~ buffers 41, ~~where~~ the delay time of each of which is 1 nanosecond ~~nano second~~. Thus, the delay circuit 33 can delay the drive signal and the sample hold signal by arbitrary time length, respectively, depending on the control by the control microprocessor 26.

Next, the effect of this embodiment will be described.

Please replace the paragraph beginning at page 9, line 6, with the following rewritten paragraph:

The imaging signal obtained in the CCD 16 driven by the drive signal is given to the CDS circuit 24 through the corrugating circuit 17, the signal cable 13 and the preamplifier 13. Also, ~~The~~ the sample hold signal output from the SSG 32 is delayed by the delay circuit 33 to be

given to the CDS circuit 24. Here, the control microprocessor 26 sets the selector circuit 42 in the delay circuit 33 delays the sample hold signal for the value set at the set switch 28.

B3 The video signal obtained in the CDS circuit 24 is converted by the A/D converter circuit 25 to a digital video signal. This digital video signal is performed each kind of video signal processing by the video signal processing circuit 34. It is converted to a video signal, which can be displayed on a monitor, to be ~~outputby~~ output by the digital encoder 35.